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Guidelines for Successful Simulation Setup

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This tutorial provides a review of the choices an engineer must make to obtain succesful results from circuit simulation

The rewards of simulation include more robust designs and faster product time to market. The cost of simulation typically includes the time spent to set up the software to perform meaningful analyses, and access to appropriate component models. This article focuses on lowering the setup barrier so that simulations yield accurate and useful results more quickly.

What is Modeling?

Component modeling involves finding parameter values for a fixed model used in a simulation to reproduce the behavior of the given device. Typically, model accuracy is compared against the measured data of the device. When the simulated and measured data are close to each other, it is said that the model is a good fit. A good model allows the designer to make accurate predictions about the component in any given application.

Models are generally a set of equations that emulate the component behavior. The model equations are hard coded into the simulator. The designer accesses the model through a set of predefined parameters (called model parameters). The process of model parameter values adjustment, so that measured data and simulated data have a good fit, is known as model parameter extraction.

The component models needed for electronic design can be grouped into two areas: discrete linear (for example, R, L, C) and nonlinear (for example, BJT, MOSFET) components; and high frequency distributed components (for example, microstrip transmission lines).

In a perfect world the designer is expected to strictly cover all interactions between components in the simulation. This type of simulation would only be possible using EM (electromagnetic) solvers, due to the need to apply Maxwell's equations (including discrete components), which is regarded as too slow, and an "overkill." The answer to this conflict is the use of circuit simulators with simplified models (sometimes called compact models). The SPICE (Simulation Program with Integrated Circuit Emphasis) circuit simulator is probably the one most designers are familiar with. Still today, after more than three decades since it was first introduced at the University of California at Berkeley, many consider it the standard in circuit simulation. SPICE requires a text file (a netlist) to describe the circuit and analyses to be performed.

Model Classes

The component models used for circuit simulation can be divided into several different classes. The model classes are:

1. *Physical models.* The model equations of this class are based on the device physics. In a good physical model all parameters will have a physical meaning. Experience teaches us that pure physical models may not be 100 percent practical (see Empirical Models).
2. *Tabular models.* In this model the measured values are used without the use of model equations. The values stored are, for example, the drain current at different bias or small signal parameters. The simulator then looks up the values and uses interpolation functions for computing values in

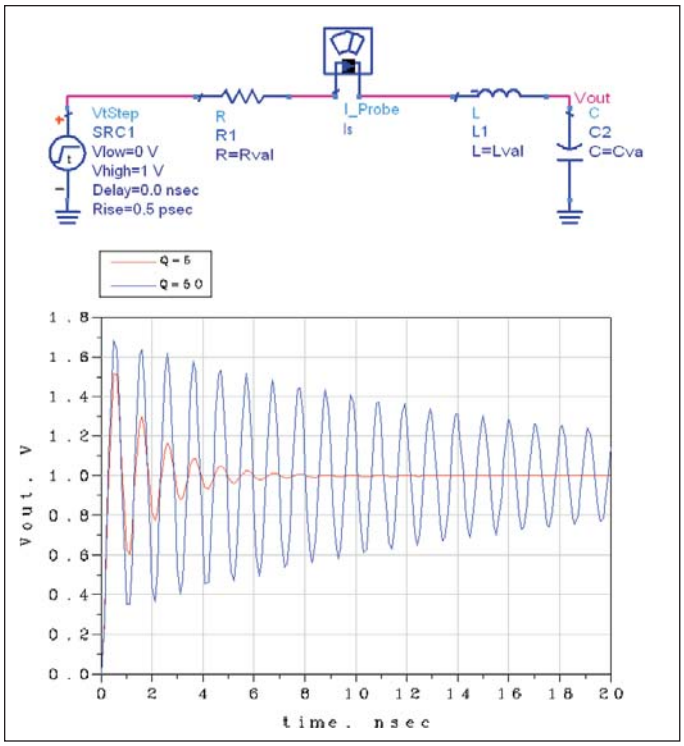

Figure 1 · Time-domain analysis of a passive circuit.

between the measurements. The advantage of tabular models is that it can provide a model when physical or empirical models are not defined or fail due to the complex nature of their equations.

3. *Empirical models.* This model formulation is totally dependent on the fitting of parameters to measurement data via curve fitting. The model parameters are the coefficients, exponents, etc. used in the curve fitting algorithm and have no physical meaning. Empirical models are valid only in the physical area at which measurements were taken during parameter extraction. This is an important limitation as compared with physical models. Fully empirical models are hardly ever used. These empirical expressions are commonly used with table models to help with the interpolation, or in physical models, when the physics does not arrive at a closed form expression or the expression requires excessive computational resources.
4. *EM models.* The need to include layout effects is demanded at higher frequencies and with smaller form factors. EM models are used increasingly as computer speed and computing power increase. This type of model is actually the EM analysis of the layout with the data imported into the simulation, similar to a tabular model. A major advantage for the design engineer is to include the effects of the layout during the design process—before the first prototype is built and layout parasitics are discovered to have an adverse effect.

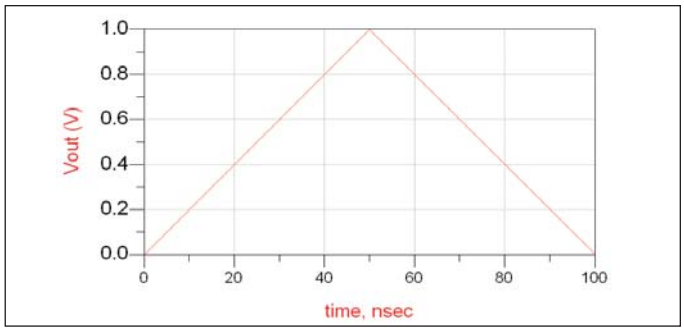

Figure 2 · Incorrect square wave sampling results.

Time Domain Simulation

Time Domain Simulations solve a set of integro-differential equations that express the time dependence of the currents and voltages of the circuit. The result of this type of analysis is nonlinear with respect to time and is similar to the measurements made by an oscilloscope. In order to obtain meaningful results from a time simulation the user must understand the time settings. The simulation time step and time stop are important parameters that need to be specified because, for commercial simulators, the other parameter default values will work in most cases.

In many applications the time stop needs to be setup so that the circuit being analyzed reaches steady state. This setting can be frustrating to novice designers, especially for circuits that have a long settling time when compared to the time step being used. This is illustrated through a simple example. In Figure 1 we analyzed the same circuit twice with the same time stop and time step. The only difference between both simulations is that we increased the value of the inductance such that the Q of the circuit at the natural frequency is 10 times larger for the second simulation. The results clearly show that with the higher Q it will take the circuit much longer (actually 10 times longer) to settle.

The time step determines the sampling rate of the time domain simulation. In the strict sense we want to use the Nyquist sampling criterion. The Nyquist rate (F_s) is in theory a sufficient condition for an analog signal to be reconstructed from a set of uniformly spaced set of time samples. If the maximum frequency of interest is F_m then the Nyquist rate is:

$$F_s = 2F_m$$

Let us examine what exactly F_m means with an example. For example say that we feed the circuit of Figure 1 with a 10 MHz square signal. It is tempting to sample at twice the 10-MHz signal frequency. These results are shown in Figure 2.

These results should not surprise us since we are only taking two samples per cycle in a signal that has a fun-

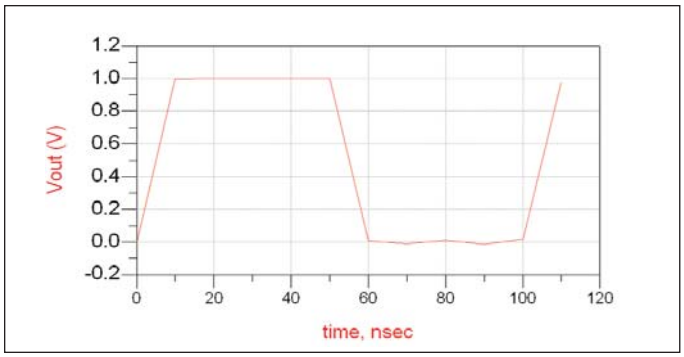

Figure 3 · Square wave fixed sampling.

damental period of 100 ns. The results are not the square wave we expected, however the simulator is doing exactly what we requested. The real problem is that we have misinterpreted what "maximum frequency of interest" means. Fourier analysis tells us that such a square wave is represented by a series of sinusoidal components that are harmonically related. Let's say we are willing to accept up to the 5th harmonic in our simulation, if so we need to sample at 100 MHz (10-ns time step). The results are shown in Figure 3 and seem to represent our signal much better. However from our prior analysis we saw that the circuit has a natural frequency of 1 GHz (set up that way intentionally), yet we do not see this effect in Figure 3. The reason again is we have not sampled this circuit well enough; fortunately circuit simulators have a more robust time step control method for this kind of problem than the one we have been using so far.

Time domain simulator engines can use one of several Time Step Control methods. Hence when setting up a time simulation the Time Step Control method needs to be known as well. The Time Step Control method being used so far is the "Fixed" method. In a Fixed Time Step Control simulation the time step is constant throughout the entire simulation and places all the responsibility on the user to select an appropriate time step value. The default method typically used is called "Truncation Error." The Truncation Error method uses the current estimate of local truncation error to determine an appropriate time step. The bottom line (without going into much technical detail) is that Truncation Error is an adaptive time step control method; the user needs to set the maximum time step to be used. Now let's switch the time step control method in our analysis. The results are shown in Figure 4. Notice that the results are what we expect from our a priori knowledge of the circuit and circuit excitation. In Figure 4 we have also plotted the time step used by the simulator in the analysis. We note that the time step adapts as the simulation is performed. It is quite impressive to see that the Truncation Error method sets a finer time increment during the transient portion

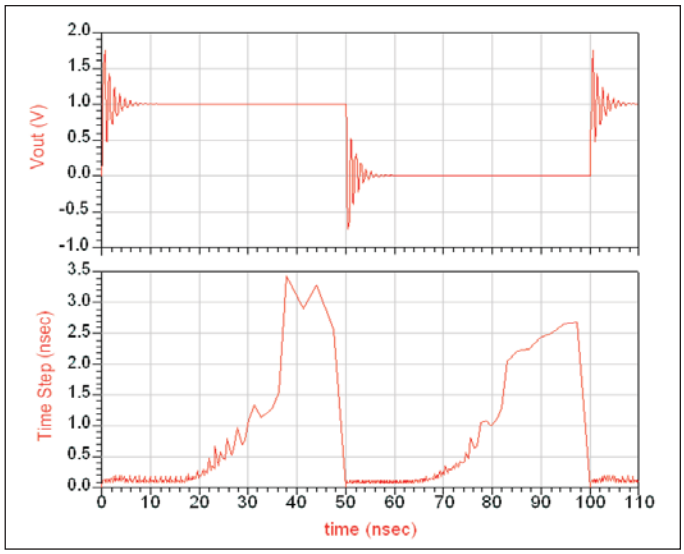

Figure 4 · Square wave Tuncation Error Time Step Control.

of the response and increments as the response gets into steady state.

The Truncation Error method is the default time step control method in SPICE and many commercial simulators. At this point the reader may think, "why even consider any other method since this method will correctly sample the circuit response?" The reality is that no method can cover all applications. Designers with more experience can tell you how frustrating the "time step too small" error message can be. When encountering this kind of convergence problem one can try another time step control method (either fix or iteration count). There are other remedies that will depend on the type of application being analyzed. For example, when analyzing a bistate circuit, an initial condition may need to be specified on the output nodes because the solution may not be clearly defined from the topology before it starts the simulation. The analysis of non-linear circuits (such as amplifiers, multipliers, and so on) can also lead to convergence issues, especially if driven into compression. Frequently, these circuits will successfully simulate if you do not start them at the full signal level. In other words, start the simulation at a power level at which the circuit converges and increase the power level with simulation time.

Frequency Domain Simulations

The frequency response of a circuit is also of great interest to designers and points out the need for frequency domain simulation engines. Frequency domain simulations are done under steady state conditions. We divide the frequency domain analysis in terms of linearity; hence there exists linear and non-linear frequency domain simulation engines.

Frequency Domain Linear Simulation

In SPICE and many other popular simulation programs there is an AC analysis which is a linear frequency-domain simulator. The AC analysis will produce the amplitude and phase of the current or voltage response of the circuit being analyzed. Also, many popular RF simulation programs will include an S-parameter simulation analysis; typically any arbitrary n-port circuit can be analyzed.

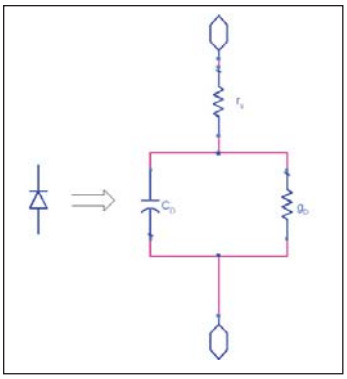

Figure 5 · Diode small signal model.

In these types of simulations any kind of active component is replaced by its small signal equivalent circuit. In essence the circuit will not include large signal effects. To better understand this analysis, Figure 5 shows the equivalent small signal model used in SPICE for a diode, where C_D is the diode intrinsic capacitance, g_D is the diode conductance, and r_s is the diode contact ohmic resistance.

The values of g_D and C_D are both determined from the DC operating point of the diode. The values determined from the DC operating point for a typical diode are shown in Figure 6 to further illustrate this point. This means that a DC analysis needs to be performed before any linear frequency domain simulation (happens in the background typically without user intervention).

Another result of using the small signal model for all active devices is that the circuit frequency response will not be sensitive to the excitation signal level. To further show the effects of this we simulated the circuit shown in Figure 7 using an AC analysis. The simulation can be executed at any signal level desired and the frequency response ($H(f) = V_{out}/V_{in}$) will always be the same, which happens since we are using the small signal equivalent model based on the DC operating point. The results also show that the response is sensitive only to the DC level of the circuit, which is controlled by the value of V_{cc}.

Frequency Domain Non-Linear Simulation

We mentioned previously that the results of a Time Domain simulation are non-linear with respect to time. This means that if we want to know the frequency content (for example, harmonics) we just need to use a Fourier Transform on the time data. While this last statement is true it comes at the expense of simulation time and computer resources for many of the typical RF analyses.

Let us consider a mixer stage in which the local oscillator frequency and radio frequency are in the GHz range and the IF is 1.0 MHz. For such an analysis we need a

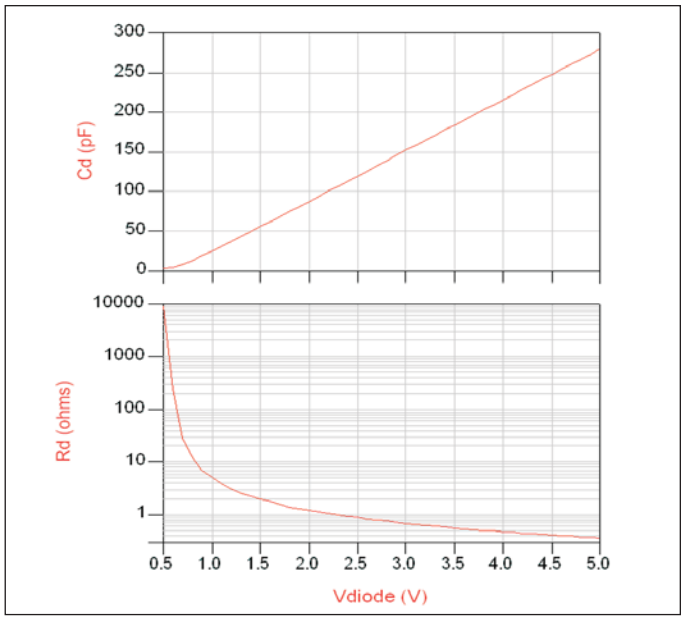

Figure 6 · Diode small signal model parameter values.

sampling rate let's say of 10 GHz at least, which means we would have a sampling period of 100 ps. Now the selection of the time stop not only has to consider the fact that we need to ensure steady state has been reached but that sufficient time samples have been collected to represent our much lower IF frequency. The period of the IF is 1 µs

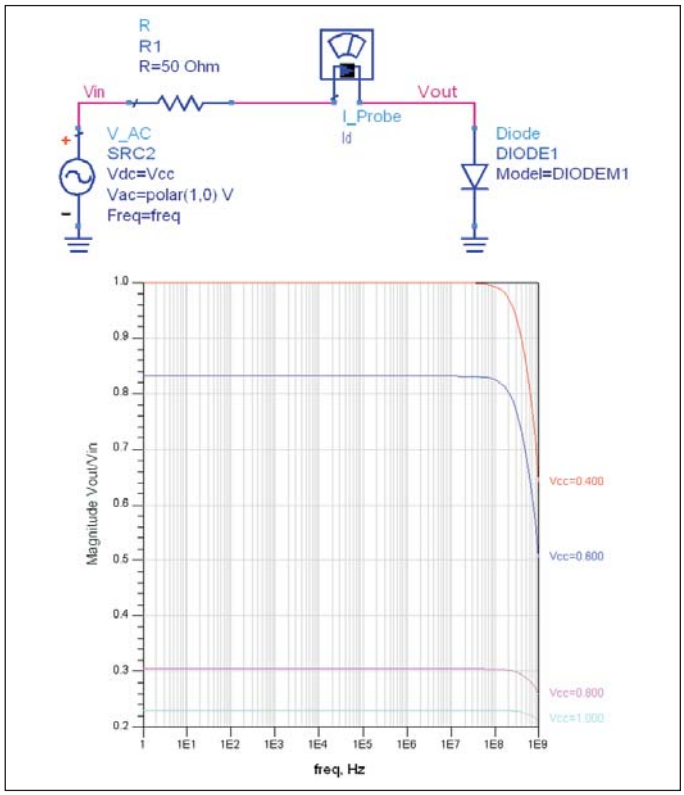

Figure 7 · Diode circuit AC results versus DC voltage.

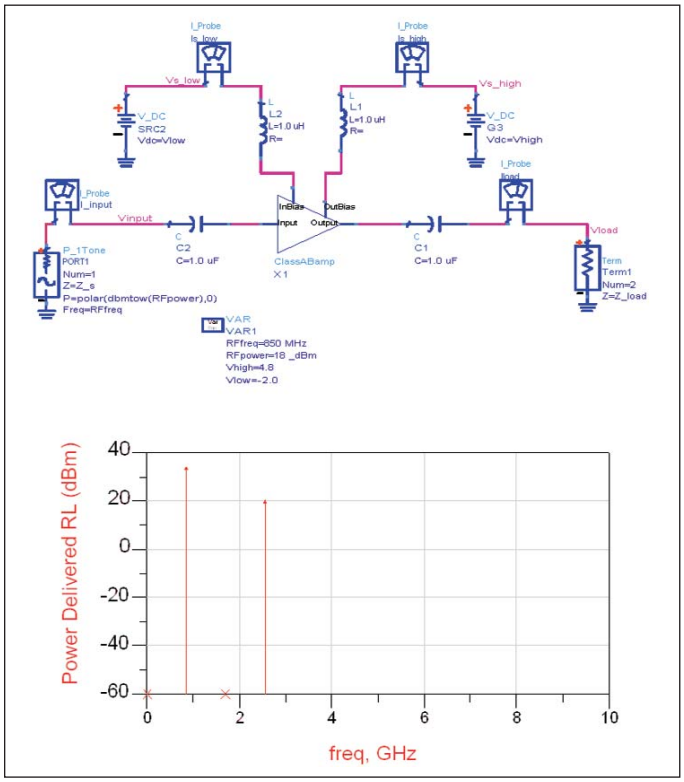

Figure 8 · Amplifier non-linear simulation.

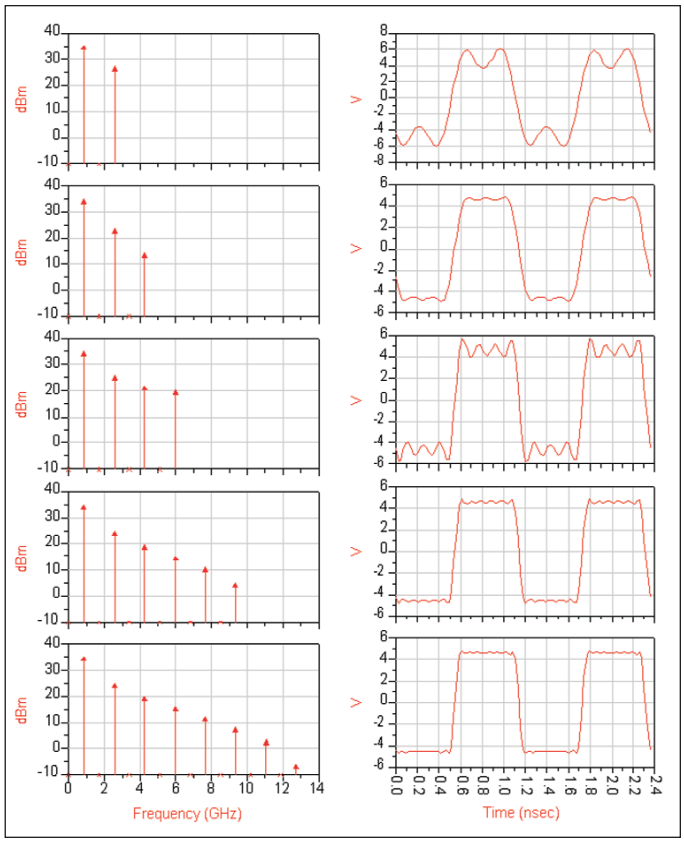

Figure 9 · Amplifier harmonic balance results versus order.

which at a sampling period of 100 ps represent 10,000 points of a steady state signal for only 1 cycle of the IF signal to be sampled.

The use of a time-domain simulator on a discrete tone analysis like the preceding example is often considered overkill, especially when you can use a simulator such as harmonic balance to solve this problem. In a harmonic balance simulation (as well as with other nonlinear frequency simulators) the user specifies the frequency tones and the order (number of harmonics and intermodulation products) to be considered in the simulation. In a harmonic balance simulation what is taking place is a truncated Fourier analysis.

Setting the order of the simulation up front can be intimidating, especially if you are a new user of harmonic balance analysis. Let us start by looking at the output of a single tone HB (harmonic balance) simulation. The amplifier in Figure 8 is a Class AB power amplifier designed to work at 850 MHz.

Examining the results, we notice that there is no DC term since the output is AC coupled. The absence of the 2nd harmonic is due to the push-pull configuration used in this design. In general, we will not see any even harmonics at the output of this circuit. We can only see up to the 3rd harmonic (3*850 MHz) because this is the order that was specified in the HB simulation.

Setting the order is not always the most straightforward task. Harmonic balance results are obviously sensitive to the order and it must be selected properly. The first indication of the order to be used is the level of nonlinearity expected. When expecting weak non-linearity a default order equal to three may work just fine. The resulting spectrum can help also to determine the order. When looking at the harmonics, if the highest harmonic is at least 40 dBc from the fundamental then it is said that the contributions of any higher harmonics can be safely ignored assuming monotonically power decreasing higher harmonics. The problem with this figure of merit is that one tends to focus the attention at the output nodes and forgets about the internal nodes in the circuit. In Figure 9 we show the output spectrum as a function of order for the circuit shown in Figure 8. Observe that the 15th harmonic is better than 40 dBc and the time domain representation of such a signal no longer shows much change. One can infer that the 15th harmonic and higher have negligible impact on the output signal.

While looking at the harmonics and time waveforms gives the designer valuable information, there may be other parameters that are of greater significance. In a power amplifier the designer is probably more concerned with the accuracy of the fundamental output power (P_{out})

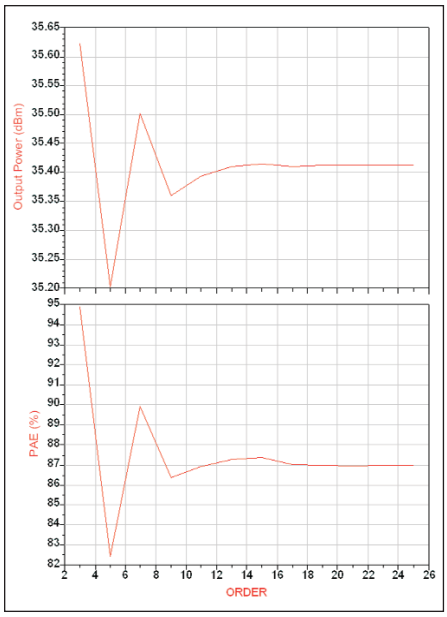

Figure 10 · Amplifier output power and PAE versus order.

and the Power Added Efficiency (PAE). In Figure 10 we show these two important parameters against the simulation order. We observe that an order = 17 converges on to the solution and any further increases in order do not show any significant change in any of these values. However, there is always a tradeoff when it comes to setting the order in terms of accuracy versus computer resources and simulation time. The higher the HB simulation order the greater the accuracy but the longer the simulation will take to complete and the more memory it will need. In the case under consideration, if the simulation time were long the designer can tweak his design at a lower order (for example, order = 9) just to get results in a faster timeframe while adjusting design parameters and then simulate the final design at a higher order (for example, order = 21) for very accurate results.

Oscillator Example

The schematic in Figure 11 shows a basic LC oscillator designed to work at 1 GHz.

This circuit can be analyzed using either harmonic balance or time domain analyses. If we are interested in performing a startup analysis then the proper simulator would be a time analysis engine (be prepared to wait for the results if you are simulating a high Q oscillator such as one using a crystal). The startup results for this circuit are shown in Figure 12.

The same circuit when analyzed with harmonic balance will produce the fundamental oscillating frequency components and the harmonics as specified in the analysis. The results of the HB analysis of this circuit are

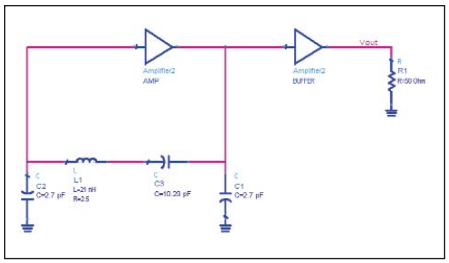

Figure 11 · 1.0-GHz oscillator circuit example.

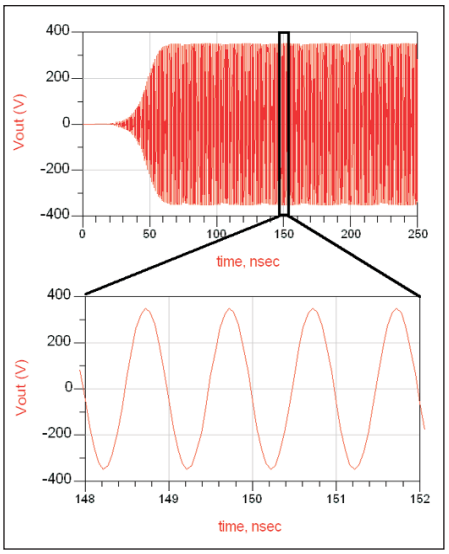

Figure 12. Oscillator time domain results.

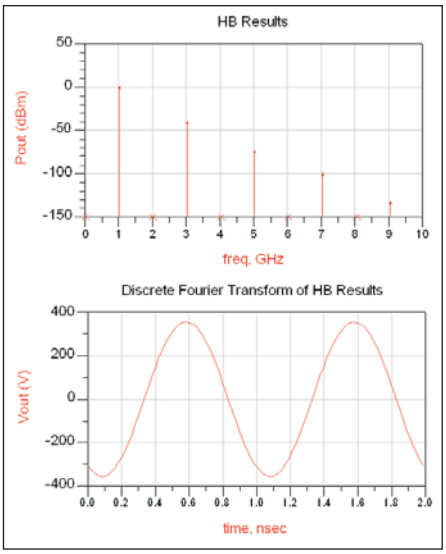

Figure 13 · Oscillator harmonic balance results.

shown in Figure 13.

From the time analysis results we could determine the frequency spectrum by applying a Fourier Transform to the steady state part of the signal. If this is the case then why would we want to bother with a harmonic balance simulation when a time domain simulation might give us all the information we need? There are several reasons, including (1) computer resources needed for the analysis and (2) simulation time. The time domain analysis requires more data to be saved in order to provide meaningful results, in this analysis the time domain saved 4501 points for the output data and the HB simulation only saved 10 points (times 2 since the results of HB are complex in nature, e.g., magnitude and angle).

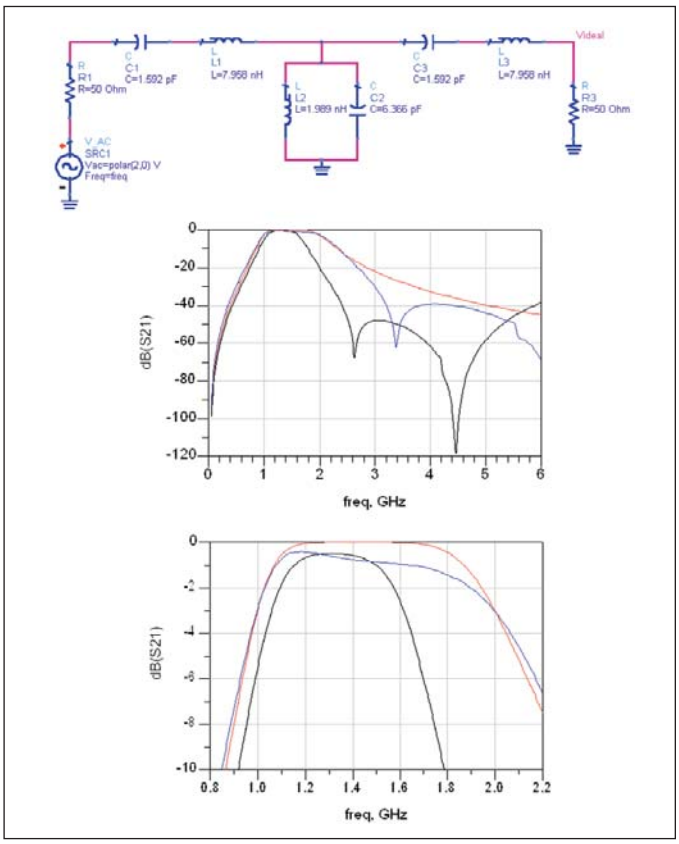

Figure 14 · Butterworth bandpass filter circuit and frequency response.

	Ideal Value (Red)	Initial Selection (Black)	Optimized Value (Blue)
C1	1.592 pF	1.5 pF	1.7 pF
L1	7.598 nH	8.2 nH	4.7 nH
C2	6.366 pF	6.2 pF	3.9 pF
L2	1.989 nH	1.8 nH	2.7 nH
C3	1.592 pF	1.5 pF	1.7 pF
L3	7.598 nH	8.2 nH	4.7 nH

Table 1 · Butterworth bandpass filter component values.

This shows the ability of HB to handle larger problems with the same limited amount of computer resources (e.g., available RAM). The simulation duration for the time domain analysis is also an important consideration. The fact that a time analysis runs so many iterations can represent a total simulation time that can be many orders higher of a corresponding HB analysis (depending on the complexity and nonlinear characteristics of the circuit).

Bandpass Filter Example

The following filter (shown in Figure 14) is a Butterworth filter designed using the standard synthesis equations. The frequency response from this circuit is the red trace shown in the chart. We note that the 3-dB frequencies are 1 GHz and 2 GHz as per the design. However, if one were to build this filter the part values are not standard vendor values.

Therefore we need to select from our vendor parts the capacitors and inductors that closely resemble the ideal values. The black trace in the response curves shows the initial replacement of the ideal parts with vendor modeled parts. These values were selected to be the closest standard value to the ideal value. This initial selection resulted in very poor frequency response since it has been altered and does not resemble the original response. The blue trace, on the other hand, matched the ideal response very closely in the vicinity of the band of interest. These final values were obtained by optimizing the design using the vendor models. Table 1 shows values used for the different response shown in Figure 14.

This experiment shows that the accuracy of the models is very important. RF engineers know that passive devices will have parasitics that need to be included in the design process for final design to work. Notice that the ideal filter included no losses, while both designs with vendor models include losses. The final design will also need to consider the PCB parasitic effects on the response; this can be done using an EM simulator to analyze the PCB by itself and running the circuit simulation including the EM results as an input to the simulation (for example, electromagnetic cosimulation).

Summary

This article has focused on the selection and setup of different simulation engines available in the CAD space today. Ultimately, the design requirements will dictate the kind of analysis that needs to be performed. Analysis setup is the key to obtaining useful and accurate results from your simulations. Device models are simulation inputs and these need to be a good fit to the actual device performance they are trying to emulate. The simulations discussed in this article were performed using Advanced Design System (ADS2004A) from Agilent Technologies, Inc. (www.agilent.com/find/eesof).

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